Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-5. (Cancelled)

6. (Currently Amended) A method for producing a semiconductor device having a cylindrical storage node comprising a bottom portion and a cylindrical portion which surrounds an outer circumference of said bottom portion and extends upward, which comprises the steps of:

forming a contact hole which penetrates an interlayer insulating film formed on a semiconductor substrate;

forming an electric conductive film on said interlayer insulating film whereby said contact hole is filled to obtain a contact to said substrate;

forming an insulating film on said electric conductive film;

patterning by an anisotropic etching said insulating film and said electric conductive film to form a configuration corresponding to said cylindrical portion so that [[the]] a core and the bottom portion of said cylindrical portion are formed;

forming the cylindrical portion on the side of said core and said bottom portion wherein an outer wall of said cylindrical portion is roughened, comprising the sequential steps of forming a film containing silicon on said core and said bottom portion; roughening an outer surface of said film containing silicon by forming silicon grains in the outer surface

of it; and conducting an anisotropic etching for patterning to form ~~a side-wall like~~ said cylindrical portion having a side-wall like shape at the side of said core and said bottom portion;

removing said core;

forming a dielectric film to cover said cylindrical storage node comprising said cylindrical portion and said bottom portion; and

forming a cell plate on said dielectric film, whereby a capacitor constituted by said cylindrical storage node, said dielectric film and said cell plate is formed.

7. (Currently Amended) A method for producing a semiconductor device having a cylindrical storage node comprising a bottom portion and a cylindrical portion which surrounds an outer circumference of said bottom portion and extends upward, which comprises the steps of:

forming a contact hole which penetrates an interlayer insulating film formed on a semiconductor substrate;

forming an electric conductive film on said interlayer insulating film whereby said contact hole is filled to obtain a contact to said substrate;

forming an insulating film on said electric conductive film;

patterning by an anisotropic etching said insulating film and said electric conductive film to form a configuration corresponding to said cylindrical portion so that [[the]] a core and the bottom portion of said cylindrical portion are formed;

forming the cylindrical portion on the side of said core and said bottom portion wherein an outer wall of said cylindrical portion is roughened, comprising forming an

amorphous silicon film on said core and said bottom portion; conducting an anisotropic etching of said amorphous silicon film to form ~~a side wall like~~ said cylindrical portion having a side-wall like shape at the side of said core and said bottom portion; and roughening [[an]] said outer wall [[surface]] of said cylindrical portion ~~amorphous silicon~~ by forming silicon grains ~~in the outer surface of it to thereby form said cylindrical portion~~;

removing said core;

forming a dielectric film to cover said cylindrical storage node comprising said cylindrical portion and said bottom portion; and

forming a cell plate on said dielectric film, whereby a capacitor constituted by said cylindrical storage node, said dielectric film and said cell plate is formed,

wherein the inner wall of the cylindrical portion having [[a]] the roughened outer wall is constituted by amorphous silicon.

8. (Currently Amended) A method for producing a semiconductor device according to Claim 6, wherein the roughening of the outer surface of the film containing silicon is selected from the group consisting of a heat treatment with use of silane and a heat treatment in vacuum after a treatment to the outer surface of said film containing silicon with use of hydrofluoric acid, whereby projections and recesses are formed in the outer surface [[wall]] of said [[amorphous]] film containing silicon by forming silicon grains in the outer surface [[wall]].

9. (Currently Amended) A method for producing a semiconductor device according to claim 7, wherein the roughening of the outer wall [[surface]] of the cylindrical

portion ~~amorphous silicon~~ is selected from the group consisting of a heat treatment with use of silane and a heat treatment in vacuum after a treatment to the outer wall [[surface]] of said cylindrical portion ~~amorphous silicon~~ with use of hydrofluoric acid, whereby projections and recesses are formed in the outer wall of said cylindrical portion ~~amorphous silicon~~ by forming silicon grains in the outer wall.

10. (Currently Amended) A method for producing a semiconductor device according to Claim 8, wherein the inner wall of the cylindrical portion having [[a]] the roughened outer wall is constituted by said film containing silicon, said film containing silicon including amorphous silicon.

11. (Cancelled)

12. (Currently Amended) A method for producing a semiconductor device having a cylindrical storage node comprising a bottom portion and a cylindrical portion which surrounds an outer circumference of said bottom portion and extends upward, which comprises steps of:

forming a contact hole which penetrates an interlayer insulating film formed on a semiconductor substrate;

forming an electric conductive film on said interlayer insulating film whereby said contact hole is filled to obtain a contact to said substrate;

forming an insulating film on said electric conductive film;

patterning by an anisotropic etching said insulating film and said electric conductive film to form a configuration corresponding to said cylindrical portion so that [[the]] a core and the bottom portion of said cylindrical portion are formed;

forming the cylindrical portion on the side of said core and said bottom portion wherein an outer wall of said cylindrical portion is roughened;

forming a dielectric film on said cylindrical storage node comprising said cylindrical portion and said bottom portion within which said core remains; and

forming a cell plate on said dielectric film, whereby a capacitor constituted by said cylindrical storage node, said dielectric film and said cell plate is formed.

13. (Currently Amended) A method for producing a semiconductor device according to Claim 12, wherein the step of forming the cylindrical portion on the side of the core and the bottom portion wherein the outer wall of the cylindrical portion is roughened, comprises forming an amorphous silicon film on said core and said bottom portion; roughening an outer surface of said amorphous silicon film by forming silicon grains in the outer surface of it; and conducting an anisotropic etching for patterning to form ~~a side-wall like~~ said cylindrical portion having a side-wall like shape at the side of said core and said bottom portion.

14. (Currently Amended) A method for producing a semiconductor device according to Claim 12, wherein the step of forming the cylindrical portion on the core and the bottom portion wherein the outer wall of the cylindrical portion is roughened, comprises forming an amorphous silicon film on said core and said bottom portion; conducting an

anisotropic etching of said amorphous silicon film to form ~~a side-wall like~~ said cylindrical portion having a side-wall like shape at the side of said core and said bottom portion; and roughening [[an]] said outer wall [[surface]] of said cylindrical portion ~~amorphous silicon~~ by forming silicon grains ~~in the outer surface of it to thereby form said cylindrical portion~~.

15. (Currently Amended) A method for producing a semiconductor device according to claim 13, wherein the roughening of the outer surface of the amorphous silicon film is selected from the group consisting of a heat treatment with use of silane and a heat treatment in vacuum after a treatment to the outer surface of said amorphous silicon film with use of hydrofluoric acid, whereby projections and recesses are formed in the outer surface [[wall]] of said amorphous silicon film by forming silicon grains in the outer surface [[wall]].

16. (Currently Amended) A method for producing a semiconductor device according to claim 14, wherein the roughening of the outer wall [[surface]] of said cylindrical portion ~~amorphous silicon~~ is selected from the group consisting of a heat treatment with use of silane and a heat treatment in vacuum after a treatment to the outer wall [[surface]] of said cylindrical portion ~~amorphous silicon~~ with use of hydrofluoric acid, whereby projections and recesses are formed in the outer wall of said cylindrical portion ~~amorphous silicon~~ by forming silicon grains in the outer wall.

17. (Currently Amended) A method for producing a semiconductor device according to claim 15, wherein the inner wall of the cylindrical portion having [[a]] the roughened outer wall is constituted by amorphous silicon.

18. (Currently Amended) A method for producing a semiconductor device according to claim 16, wherein the inner wall of the cylindrical portion having [[a]] the roughened outer wall is constituted by amorphous silicon.

19. (New) A method for producing a semiconductor device having a cylindrical storage node comprising a bottom portion and a cylindrical portion which surrounds an outer circumference of said bottom portion and extends upward, which comprises the steps of:

forming a contact hole which penetrates an interlayer insulating film formed on a semiconductor substrate;

forming an electric conductive film on said interlayer insulating film whereby said contact hole is filled to obtain a contact to said substrate;

forming an insulating film on said electric conductive film;

patterning by an anisotropic etching said insulating film and said electric conductive film to form a configuration corresponding to said cylindrical portion so that a core and the bottom portion of said cylindrical portion are formed;

forming the cylindrical portion on the side of said core and said bottom portion wherein an outer wall of said cylindrical portion is roughened, comprising the sequential steps of forming a film containing silicon on said core and said bottom portion; roughening

an outer surface of said film containing silicon by forming silicon grains in the outer surface of it; and conducting an anisotropic etching for patterning to form said cylindrical portion having a side-wall like shape at the side of said core and said bottom portion;

removing said core;

forming a dielectric film to cover said cylindrical storage node comprising said cylindrical portion and said bottom portion; and

forming a cell plate on said dielectric film, whereby a capacitor constituted by said cylindrical storage node, said dielectric film and said cell plate is formed.

wherein the inner wall of the cylindrical portion having the roughened outer wall is constituted by said film containing silicon, said film containing silicon including amorphous silicon.

20. (New) A method for producing a semiconductor device according to Claim 7, wherein the anisotropic etching of said amorphous silicon is conducted so as to cover whole circumferential areas of said core and said bottom portion by said cylindrical portion, and whole the outer wall of the cylindrical portion covering the whole circumferential areas of said core and said bottom portion is roughened.

21. (New) A method for producing a semiconductor device having a cylindrical storage node comprising a bottom portion and a cylindrical portion which surrounds an outer circumference of said bottom portion and extends upward, which comprises the steps of:

forming a contact hole which penetrates an interlayer insulating film formed on a semiconductor substrate;

forming an electric conductive film on said interlayer insulating film whereby said contact hole is filled to obtain a contact to said substrate;

forming an insulating film on said electric conductive film;

patterning by an anisotropic etching said insulating film and said electric conductive film to form a configuration corresponding to said cylindrical portion so that a core and the bottom portion of said cylindrical portion are formed;

forming the cylindrical portion on the side of said core and said bottom portion wherein an outer wall of said cylindrical portion is roughened, comprising forming an amorphous silicon film on said core and said bottom portion; conducting an anisotropic etching of said amorphous silicon film to form said cylindrical portion having a side-wall like shape at the side of said core and said bottom portion so as to cover whole circumferential areas of said core and said bottom portion by said cylindrical portion; and roughening whole said outer wall of said cylindrical portion covering the whole circumferential areas of said core and said bottom portion by forming silicon grains;

removing said core;

forming a dielectric film to cover said cylindrical storage node comprising said cylindrical portion and said bottom portion; and

forming a cell plate on said dielectric film, whereby a capacitor constituted by said cylindrical storage node, said dielectric film and said cell plate is formed.

22. (New) A method for producing a semiconductor device according to Claim 12, wherein the step of forming the cylindrical portion on the side of the core and the bottom portion wherein the outer wall of the cylindrical portion is roughened, comprises the sequential steps of forming an amorphous silicon film on said core and said bottom portion; roughening an outer surface of said amorphous silicon film by forming silicon grains in the outer surface of it; and conducting an anisotropic etching for patterning to form said cylindrical portion having a side-wall like shape at the side of said core and said bottom portion.

REMARKS

As indicated in the Advisory Action dated September 29, 2003, the proposed claim amendments dated July 21, 2003 were not entered. In response, Applicants has filed this Amendment together with a Request for Continued Examination. Currently, claims 6-10 and 12-18 are pending, all of which remain rejected.

First, Applicants acknowledge, with appreciation, Examiner Maldonado's courtesy and professionalism in responding to Applicants' inquiries on October 3 and 6, 2003. It is Applicants' understanding that the §112, first paragraph rejection has been withdrawn based on the Applicants' July 21, 2003 response, and the §103 rejection of claim 6 might be overcome if claim 6 is amended in the same manner as in the July 21, 2003 Amendment.

In this Amendment, claims 6-10 and 12-18 have been amended, and new claims 19-22 have been added. Specifically, claim 6 has been amended to include the limitation "comprising the sequential steps of forming a film containing silicon…; roughening an outer surface of said film… ; and conducting an anisotropic etching…." Adequate descriptive support for the amendment can be found in, for example, the second full paragraph at page 16 of the specification.

New claims 19 has been prepared based on a combination of claims 6 and 10. Adequate support for new claims 20 and 21 can be found in, for example, Figs. 4(a) and 4(b). New claim 22 is supported in, for example, the second full paragraph at page 16 of the specification.

Cosmetic amendment has also been made to claims 6-10 and 12-18 to improve wording and remove possible antecedent basis issues. No new matter is introduced.

The Examiner pointed out that the amendments to claim 7 were not cosmetic and would not be entered because "the claim recites roughening the outer sidewall of the amorphous silicon layer, further limiting the claim" (see the last four lines in the second full paragraph at page 2 of the Advisory Action). In this Amendment, claim 7 has been amended in the same way as in the July 21, 2003 Amendment. Applicants stress that the scope of claim 7 is not limited by such amendments because the recitation "roughening said outer wall of the cylindrical portion" (after amendment) is not lesser in scope than "roughening an outer surface of said amorphous silicon" (before amendment), within the context of the claim.

Applicants hereby respectfully request that the Examiner clarify the record by acknowledging the claim for foreign priority and receipt of the certified copies of the priority documents filed in Serial No. 09/086,752 on May 29, 1998.

Claims 6-10 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hsieh et al. in view of the applicants admitted prior art ("AAPA") in the instant application and DeBoer et al.

In the statement of the rejection, the Office Action admitted that Hsieh et al. fails to teach that the configuration of the lower electrode is cylindrical. Then, the Office Action cited AAPA (Figs. 6 and 7) and asserted that it teaches forming a DRAM capacitor structure in which the lower electrode (5a) is cylindrical. The Office Action further admitted that the proposed combination of Hsieh et al. and AAPA fails to expressly teach roughening the outer wall of the cylindrical storage electrode. However, the Office Action cited DeBoer et al., asserting that it teaches the step of roughening the outer wall of a storage electrode (70a).

Then, the Office Action concluded that it would have been obvious to combine the teachings of DeBoer et al. with the teachings of Hsieh et al. and AAPA to enable the roughened surface of DeBoer et al. to be formed.

Claim 6.

As mentioned above, Applicants acknowledge, with appreciation, the Examiner's indication that amendment to claim 6 may overcome the §103 rejection over prior art of record (see page 2, the first full paragraph of the Advisory Action). Applicants respectfully solicit favorable consideration of claim 6.

Claim 7.

Applicants submit that Hsieh et al., AAPA and DeBoer et al., either individually or in combination, do not teach or suggest the limitation "the inner wall of the cylindrical portion having the roughened outer wall is constituted by amorphous silicon." This is so because DeBoer discloses a feature that the amorphous silicon layer is crystallized (column 4, lines 19-20), a feature contrary to that recited in claim 7. Moreover, it is apparent that Hsieh et al., and AAPA are silent on this limitation.

Thus, the teachings of Hsieh et al., AAPA and DeBoer et al., either individually or in combination, would not have suggested each and every limitation of claim 7. In the instant case, the pending rejection has not established *prima facie* obviousness of the claimed invention as recited in claim 7, because the proposed combination fails to satisfy the all claim limitations standard required under §103. *See In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Applicants, therefore, solicit withdrawal of the rejection of claim 7.

Dependent Claims 8-10.

If an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Accordingly, as claims 6 and 7 are patentable for the reasons set forth above, it is submitted that dependent claims 8-10 which respectively depend on claims 6 and 7 are also patentable. The Examiner's additional comments with respect to the claims do not cure the argued fundamental deficiencies of the proposed combination of Hsieh et al., AAPA and DeBoer et al. Applicants traverse the rejections of those claims and solicit withdrawal thereof.

Claims 12-18 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hsieh et al. in view of AAPA, DeBoer et al. and Dennison et al.

In the July 21, 2003 response, Applicants explained that there is no motivation to combine the teachings of Dennison et al. with the teachings of Hsieh et al., AAPA and DeBoer et al. In the Advisory Action, the Examiner responded, "it is well-known to leave the 'core' as claimed; followed by forming a dielectric layer and forming a capacitive plate as well as removing the core, followed by forming the dielectric layer and the capacitive plate" by citing MPEP 2144.07 (see the third full paragraph at page 2 of the Advisory Action). In response, Applicants submit that this Examiner's assertion is unreasonable because each of the references does not show a combination of the "core" and a cylindrical storage node having a roughened surface, as claimed, i.e., the claimed combination is not well known.

In the fourth full paragraph at page 2 of the Advisory Action, the Examiner further asserted as if Applicants argued that Dennison et al. teaches away from the claimed invention. In response, it is submitted that Applicants pointed out in the July 21, 2003 response that there is no requisite realistic motivation to "combine the teachings of Dennison et al. with the teachings of Hsieh et al., the prior art and DeBoer et al., to enable the core to remain over the bottom portion of the storage node of the capacitor structure" (page 8, lines 2-6 of the April 21, 2003 Office Action), but did not argue that Dennison et al. teaches away from the claimed invention.

In other words, Applicants raised the issue as to whether the Examiner did not show any realistic motivation to impel a person skilled in the art to modify the device obtained by combining Hsieh et al., AAPA and DeBoer et al., based on the teaching of Dennison et al. What Applicants argued is that (1) Dennison et al. discloses that "FIG. 19 illustrates an alternate embodiment whereby second dielectric layer 38 is not removed prior to application of the capacitor dielectric layer 48 and upper poly plate layer 50" (emphasis added) (column 6, lines 18-21); (2) However, Dennison et al. also discloses that "Removal of layer 38 is preferred to further maximize the exposed area for capacitance by utilizing the outer sides of rings 42" (emphasis added) (column 6, lines 21-23); and (3) It can therefore be considered that Dennison et al. recommends to remove the "core." Then, Applicants concluded that since Hsieh et al. and DeBoer et al. teach that the "core" is removed and Dennison et al. teaches that removal of the "core" (layer 38) is preferred, there is no requisite realistic motivation to modify Hsieh et al., AAPA and DeBoer et al. to have the "core" and the Examiner did not show any factual basis supporting such motivation.

Therefore, Applicants respectfully request the Examiner to consider whether there is any requisite realistic motivation and any factual basis supporting such motivation in prior art of record, and also solicit favorable consideration of claim 12-18. *See In re Lee*, 277 F.3d 1338, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002).

For the Examiner's information, the following is the reproduction of the Applicants' July 21, 2003 argument.

> In the statement of the rejection, the Office Action admitted that the proposed combination of Hsieh et al., AAPA and DeBoer et al. fails to teach forming a dielectric film on said cylindrical storage node comprising said cylindrical portion and said bottom portion within which said core remains. However, the Office Action newly cited Dennison et al., asserting that it teaches forming a dielectric film on a storage node comprising a sidewall portion (42) and a bottom portion (34) within which a "core" (38) remains. The Office Action then concluded that it would have been obvious to combine the teachings of Dennison et al. with the teachings of Hsieh et al., AAPA and DeBoer et al., to enable the "core" to remain over the bottom portion of the storage node of the capacitor structure. This rejection is respectfully traversed.
>
> **There is no motivation.**
>
> In imposing a rejection under 35 U.S.C. §103, the Examiner is required to make a "thorough and searching" factual inquiry and, based upon such a factual inquiry, explain **why** one having ordinary skill in the art would have been realistically impelled to modify particular prior art to arrive at the claimed invention. *In re Lee*, 277 F.3d 1338, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002). Merely identifying features of a claimed invention in disparate prior art references does not, automatically, establish the requisite motivation for combining references in any particular manner. *In re Dembiczak*, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999); *Grain Processing Corp. v. American-Maize Products Co.*, 840 F.2d 902, 5 USPQ2d 1788 (Fed. Cir. 1988).
>
> In applying the above legal tenets to this case, it is apparent that the Examiner has **not** established the requisite motivational element. The Examiner has merely pointed to the acknowledged prior art and then announced, "it would have been obvious… to combine the teachings of Dennison et al. with the teachings of Hsieh et al., AAPA and DeBoer et al., to enable the core to remain over the bottom portion of the storage node of the capacitor structure" (ultimate sentence of the paragraph bridging pages 7 and 8 of the Office Action).
>
> Applicants submit that the Office Action did not make it clear **where** the prior art discloses the motivation to combine the teachings of those references. *In re*

Lee, supra. Moreover, based on Applicants' review, Dennison et al., Hsieh et al., AAPA and DeBoer et al. do not disclose any motivation to combine their teachings.

Dennison et al. discloses that "FIG. 19 illustrates an alternate embodiment whereby second dielectric layer 38 is not removed prior to application of the capacitor dielectric layer 48 and upper poly plate layer 50" (emphasis added) (column 6, lines 18-21). However, Dennison et al. also discloses that "Removal of layer 38 is preferred to further maximize the exposed area for capacitance by utilizing the outer sides of rings 42" (emphasis added) (column 6, lines 21-23). It can therefore be considered that Dennison et al. recommend to remove the "core."

Further, Hsieh et al. and DeBoer et al. disclose a step of removing the "core," but do not disclose the "core" remains. AAPA is silent on the "core."

For example, Hsieh et al. discloses that "an oxide-dry-etching process or HF dip (stop on silicon nitride layer 40) is performed to remove the second oxide layer 51" and "FIG. 8 shows the resulting doped polysilicon structure, which serves as a bottom electrode 58 of DRAM cell capacitor with 'U shape' in cross section view" (column 4, lines 8-13). As shown in Figs. 7a and 8, Hsieh et al. discloses removing a "core" (second oxide layer) 51, but does not mention that the "core" 51 can remain there. Hsieh et al. further discloses in relation to Figs. 10a-10c showing the formation of TiN layers 62a-62c that "The sputtering process can cover a thin layer of low-resistance TiN on most flat area" and "the collimated-sputtering process can enhance the titanium nitride (TiN) formation on the bottom of deep small holes" (column 4, lines 28-38). According to these sentences, it can be considered that Hsieh et al. does not intend to have the "core" 51 in the bottom electrode 58.

DeBoer et al. discloses that "Referring to FIG. 16, support wall material laterally inwardly of outer surfaces 72a is removed, preferably through a suitable oxide etch which is conducted selectively relative to the material from which structures 70a are formed" and "Accordingly, blocks 92, 94 are removed" (column 7, lines 31-35). DeBoer et al. continues to discloses that "Subsequently, a capacitor dielectric layer 74a and an outer capacitor plate layer 76a are formed operably proximate structures 70a." (column 7, lines 36-38). DeBoer et al. also does not teach that the "core" (see blocks 92, 94) remains in the structures 70a.

Accordingly, Applicants submit that there is no motivation to combine the teachings of Dennison et al. with the teachings of Hsieh et al., AAPA and DeBoer et al., to enable the core to remain over the bottom portion of the storage node of the capacitor structure. In short, Hsieh et al. and DeBoer et al. teach that the "core" is removed, and also Dennison et al. teaches that removal of the "core" (layer 38) is preferred. No references describe the necessity to have the "core." It should, therefore, be apparent the a *prima facie* basis to deny patentability to the claimed invention has **not** been established for lack of the requisite factual basis and warranted the requisite realistic motivation. Applicants respectfully request the

Examiner to show factual basis supporting the motivation to combine those references.

New Claims 19-21.

Applicants submit that new claims 19 and 22 are patentable for the same reasons with respect to claim 6.

Further, new claims 20 and 21 recites that whole circumferential areas of the core and the bottom portion are covered by the cylindrical portion, and whole the outer wall of the cylindrical portion covering the whole circumferential areas of the core and the bottom portion is roughened by forming silicon grains. The prior art of record does not teach or suggest these limitations. In fact, as shown in, for example, Fig. 15 of DeBoer, the whole circumferential area of layer 86 which appears to correspond to the bottom portion of the claimed invention is not covered by the structures 70a having a roughened surface (outer surface) 72a. The circumferential area of the layer 86 is completely exposed and smooth in DeBoer.

Accordingly, Applicants respectfully solicit favorable consideration of those new claims.

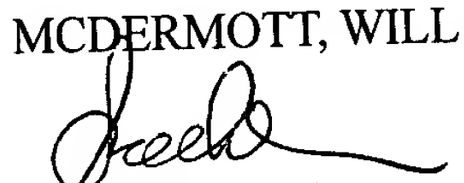
Conclusion.

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



Stephen A. Becker
Registration No. 26,527
600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 SAB:TT:lnm
Facsimile: (202) 756-8087
Date: October 21, 2003

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